

Graphene growth directly on functional substrate

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Abstract

Graphene is perhaps the most promising material ever discovered for microelectronics applications, but its preparation includes either high-temperature processing or film transfer, and sometimes both of them, which forbid for the moment its introduction into fabrication lines. In this communication we report a synthesis route involving exposure of nickel thin films deposited on silicon oxide to a mixture of methane and hydrogen activated by DC plasma at 450°C. In addition of the awaited graphene film formed at the surface of catalyst layer, we observed the formation of a second graphene film at the catalyst/silicon oxide interface. To our knowledge, no other team has yet reported graphene synthesis directly on a dielectric substrate at low temperature. With the idea of increasing the graphene structural quality, we studied the effect of additional post growth high temperature annealing. The films synthesized were characterized using Raman spectroscopy, scanning electron microscopy (SEM) and transmission electron microscopy (TEM).

Graphene synthesis; PECVD; low temperature process; Raman spectroscopy; High Resolution Transmission Electron Microscopy

Introduction

In the field of nanomaterials, a reproducible and reliable synthesis method is the most essential step to fulfill their potential. That is particularly the case for graphene. Since it was first isolated in 2004 [1], graphene has been the object of intense research [2,3] in the field of fundamental physics [4,5] as well as in the perspective of applications in low-cost large scale electronics [6], photovoltaics [7] or microelectronics [8-10]. However, good crystalline quality graphene films still lack a reliable and low-cost elaboration method. The historical micromechanical exfoliation of HOPG graphite [11,12], although yielding a good quality graphene and largely used to experimentally probe the physical properties of graphene [1,13], is not amenable to the large scale production. The CVD based methods, favored by the microelectronics industry [14] expose the sample to high temperatures, usually around 1000°C or above and always need to remove the catalyst layer used to grow graphene, implying a necessary transfer step in the process. To date, the techniques that offer the best reproducibility and produce graphene directly on substrates compatible with further processing, such as a dielectric layer, are the epitaxial growth from silicon carbide [15] or deposition from a graphene flakes suspension [16]. These two methods are not directly transferable to the microelectronics industry; the first one because it uses an expensive substrate and works at temperatures higher than 1500°C [17,18], and the latter because it only gives low-mobility films [19]. The present work is based on the central idea of preparing graphene at low temperature directly on the surface of its final substrate [20,21], using a PECVD based process. It is worth noting that the PECVD synthesis of graphene [22] normally needs high temperature (950°C). In the method reported here, graphene grows *at the interface* between the catalytic metal layer and the dielectric layer that supports it. Such an approach is the only one that avoids a film transfer that can be an important source of defects in the graphene films [23].

To the best of our knowledge, no other team has yet reported observations of such graphene growth at materials interface.

Experimental

The graphene films were prepared using plasma-enhanced chemical vapour deposition of carbon starting with a methane-hydrogen mixture as precursor gas. The exposed substrates were 200-nm nickel thin films evaporated on the 300-nm thermal oxide layer of a silicon wafer. As we grow graphene at the nickel/silicon oxide interface, we take special care to avoid surface contamination of the thermally oxidized silicon substrate prior to nickel deposition. This precaution allows us to unambiguously assert that the interface graphene is fully generated by the plasma-assisted process. Going into details, the oxidised silicon substrate is dipped into trichloroethylene (TCE) for 30 minutes, and then rinsed in acetone, 2-isopropanol (IPA), and de-ionised (DI) water. Finally, the silicon substrate is cleaned from any residual organic contamination by bathing in a $\text{H}_2\text{SO}_{4\text{conc.}}:\text{H}_2\text{O}_2$ 33% (3:1) for 30 minutes at a temperature not exceeding 150 °C. After thorough rinsing with DI water and drying with N_2 , a 200-nm nickel layer is subsequently e-beam evaporated on the substrate.

The triode plasma-enhanced CVD setup used in this study has been described elsewhere [24]. Before each deposition, the chamber is cleaned by oxygen plasma so that chamber walls do not supply uncontrolled carbon. The substrate temperature is increased with a rate of 25°C per minute in a hydrogen atmosphere. Keeping the temperature at 450°C, a pre-treatment with hydrogen plasma is performed for 2 minutes, to prevent the formation of native oxide on nickel. DC plasma is first generated in a diode setup (between the anode grid and an intermediate cathode grid) by applying a 0.17kW power to a $\text{CH}_4:\text{H}_2$ mixture (40sccm:50sccm). Pressure in

the chamber is maintained at 2 mbars during the sample exposure to plasma. Once the primary plasma is established, a 160V bias is applied to the substrate holder in order to extract reactive species from the primary plasma with 50mA intensity. After a 12 minutes plasma exposure, the chamber is allowed to cool.

Further annealing steps can be preformed under vacuum (10^{-5} mbars) in a classical CVD oven.

The sample is charged on a quartz boat, allowing its transfer from the hot zone of the oven to a much cooler one ($\sim 150^{\circ}\text{C}$) at any time. The annealing procedure is as follows: (1) the sample is transferred from the cool zone to the pre-heated hot zone (900°C) and annealed for 18 minutes. (2) The heating is then shutdown and sample allowed to slowly cool down to 750°C before (3) being quenched down to 150°C . This quenching is assumed to freeze the graphene growth and avoid the formation of thick graphene layers.

After growth and heat treatment, both the nickel surface and its interface with SiO_2 were covered by a graphene film. Nickel could then be etched using commercial nickel etchant (Nickel Etchant TBF - Transene), either for transferring the top layer graphene to other substrates, or for freeing up the interface graphene attached to the silicon oxide. Top layer graphene on nickel surface may easily attach to and get mixed with the interface graphene in this process. Accordingly, in the cases where we want to keep only the interface graphene, we applied a strong water plasma prior to the nickel etching in order to remove all carbon-based materials on the nickel surface. Figure 1 summarizes the process of film fabrication.

We analysed the structure of the films using scanning electron microscopy (SEM), for surface morphology, transmission electron microscopy (TEM) for crystallographic data, and Raman spectroscopy for crystalline quality. SEM is performed using a Hitachi S-4800 FE-SEM working at an accelerating voltage of 10 kV. TEM is performed at 120 kV using a Topcon 002B. The

cross-sectional samples for TEM are prepared by slicing and polishing using the tripod technique down to the thickness of $\sim 5\text{ }\mu\text{m}$ and then ion milling; the plan-views are obtained by etching Ni, lifting-off of the graphene membrane, and depositing it on a holey carbon grid. Raman spectra are acquired using a high-resolution (0.1 cm^{-1}) spectrometer (Labram HR800 from HORIBA Jobin Yvon) in a confocal microscope backscattering configuration. The objective used in this study is a $100\times$ ($\text{NA} = 0.9$) objective from Olympus. Excitation is provided by a tunable Ar laser from Melles Griot (514-nm wavelength). For all the Raman Stokes analysis the collection time is 5 seconds with 2 accumulations.

Results and discussion.

Figure 2 shows SEM micrographs of the different types of graphene films we synthesised during our study. We remark that, before annealing, the top and bottom films do not exhibit obvious differences, showing a continuous film on silicon oxide (bright zones on Figure 2). In contrast after annealing, the morphologies of the two films largely differs. The top films present holey but rather continuous film appearance, spotted with thick graphite inclusions, whereas the bottom film present a highly discontinuous structure.

The Raman analysis of those different films confirms the SEM observations (Figure 3). Clearly the quality of the top layer is enhanced, as the I_D/I_G ratio decreases from 1.7 to 0.8 and the I_{2D}/I_G ratio increases from 0.4 to 1.2. Concerning the interfacial graphene layer, the overall quality of the film does not change in a clear manner. In order to get a closer look at the intimate structure of the different synthesized films, a thorough analysis of the different films using high resolution transmission electron microscopy was performed.

Figure 4 shows TEM images of the samples after growth by PE-CVD at 450°C for 12 min (fig. 4a,b), and after an additional annealing treatment in vacuum at 900°C for 18 min (fig. 4c,d). Interfacial graphene is present after the two stages of treatment. It appears continuous over several tens of nm and, quite surprisingly, more so before annealing. Plan-views of the top layer films transferred on holey grids indicate that the films consist of two phases: (1) a continuous background, and (2) bulky graphite blocks. The latter have quite different shapes and structures before and after annealing: numerous with nanometre size before annealing, they are fewer but much larger after annealing. Moreover, their structure consists in pillars or onions, with (002) planes parallel to the beam before annealing (002 diffraction spots visible in fig. 4b2), while they are flat with (002) planes in the substrate plane after annealing (no 002 diffraction spots visible in fig. 4d2). On the other hand, the graphene films exhibit similar contrasts before and after annealing (but appear more sensitive to the electron beam before annealing). The selected area electron diffraction patterns (figs 4b1 and d1) show no obvious effect of the annealing on the structure of that background graphene: it appears in the two cases to consist of nano-crystalline grains, with random orientations in the plane. The line width indicates a coherence length smaller than 4 nm, which gives an order of magnitude of the size of the nano-grains. The absence of the 002 and 004 reflections confirm that the graphene crystallites are all oriented in the plane, as shown by the cross-sectional views. Figure 5 shows the structure of those nano-crystalline graphene films, as it can be deduced from the electron diffraction patterns.

Conclusion and developments

In this paper we have reported the first low-temperature synthesis of graphene films directly onto a functional substrate, namely a 300 nm thermal oxide on silicon. The process used is based on

the exposure of a nickel thin film to a carbon containing plasma at moderate temperature (450°C). Furthermore, the process allows the synthesis of a transferable film on top of the catalyst layer. As further annealing enhances the crystalline quality of the top layer film, it does not clearly affect the graphene film grown at the catalyst/silicon oxide interface. Finally, the films grown seem to be made of an arrangement of nanometric crystals rather than large crystals. As this work is still under strong development, it will now focus on the understanding of the phenomena allowing the carbon species delivered by the plasma at the surface of the catalyst to diffuse from there to the nickel/silicon oxide interface. As annealing does not seem to enhance the bottom graphene film quality, understanding these phenomena will be crucial: hopefully, it will allow us to increase the quality of the interface graphene film during the low-temperature process itself.

Figure 1. General process for plasma-assisted graphene growth.

Figure 2: SEM micrographs of the different films grown during the survey.

Figure 3. Raman spectra after PECVD (blue line) and after annealing at 900°C for 18 minutes (red line) on (a) top layer graphene, (b) interface graphene, respectively.

Figure 4. TEM images of the samples after growth by PE-CVD at 450°C for 12 min (a,b), and after an additional annealing treatment in vacuum at 900°C for 18 min (c,d). (a, c) cross-sections where graphite blocks can be seen, together with interfacial graphene in the two cases. The latter (a1, c1) appears continuous over several tens of nm, and more so before annealing. (b, d) plan-

views obtained after Ni etching, and depositing the remaining layer on a TEM holey-carbon grid. Images recorded in holey regions (no contribution of amorphous carbon). The diffraction patterns (b1 and d1) indicate that the background consists of nano-crystalline graphene, with random orientation of the nano-grains in the plane (see fig. 5). Note the absence of 002 and 004 reflections indicating a good alignment of the graphene layers in the plane. The graphite blocks are small pillars or onions, with (002) planes parallel to the beam before annealing (b2), while they are flat with no (002) planes visible after annealing (d2).

Figure 5. Schematic of the graphene structure in the plane (a) and perpendicular to the plane (b). Atomic positions in (a) are given for visualising the in-plane misorientation of four nm-sized grains; they do not represent, of course, actual positions.

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