Silicon epitaxy below 200°C: Towards thin crystalline solar cells

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ABSTRACT

Low temperature plasma processes provide a toolbox for etching, texturing and deposition of a wide range of materials. Here we present a bottom up approach to grow epitaxial crystalline silicon films (epi-Si) by standard RF-PECVD at temperatures below 200°C. Booth structural and electronic properties of the epitaxial layers are investigated. Proof of high crystalline quality is deduced from spectroscopic ellipsometry and HRTEM measurements. Moreover, we build heterojunction solar cells with intrinsic epitaxial absorber thickness in the range of a few microns, grown at 175 °C on highly doped (100) substrates, in the wafer equivalent approach. Achievement of a fill factor as high as 80 % is a proof that excellent quality of epitaxial layers can be produced at such low temperatures. While 8.5 % conversion efficiency has already been achieved for a 3.4 µm epitaxial silicon absorber, the possibility of reaching 15 % conversion efficiency with few microns epi-Si is discussed based on a detailed opto-electrical modeling of current devices.

KEYWORDS
Silicon epitaxy, RF-PECVD, low temperature, thin crystalline solar cells, modeling

1.INTRODUCTION

While huge progress were made in the history of silicon solar cells since the first patented PN junction [1], one can wonder what will be the next step for crystalline silicon (c-Si) technology. Indeed, the learning curve of c-Si solar cells has reached a plateau since 1999 with the 25% efficiency of the passivated emitter rear locally diffused (PERL) architecture [2]. More recent approaches, such as heterojunction with intrinsic thin layer (HIT), are getting closer to the same limit, with a record efficiency of 23.7% reported for 100 cm^2 cell by Sanyo [3]. However, materials and devices are close to their optimum, and very little room is left for improvement, in terms of efficiency, due to c-Si indirect band gap and non-radiative recombination processes.

Nowadays, silicon has a comfortable > 80% share of the market and it will most probably remain the dominant technology for the next decades. It is abundant, non-toxic and has a strong industrial background; consequently, cost reduction is the next challenge for TW scale. However material still represent more than 40% of the cost of c-Si PV

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modules (Ingot growth at T>1400°C, kerf loss of about 50%, etc.). Therefore innovating concepts that save materials and drive down the cost while keeping high efficiencies are very relevant. The bottom up approach of silicon epitaxy on low cost substrate or with layer transfer is promising to go way below the ~ 1$/W limit for unsubsidized large scale development. In this context, it is likely that the future of silicon cells will be based on thin crystalline films (c-SiTF) deposited or transferred on low cost substrates. Moreover, when it comes to very high efficiencies, beyond silicon limit, epitaxy is also the best approach. One can mention the remarquable results of Alta Devices getting closer to the Shockley Queisser limit, with their 28,8% for MOCVD grown GaAs signle junction solar cell reported on flexible substrate [4]. Tandem devices based on epitaxial stack of semiconductors with proper gap combination are also the solution for going further: 36.9 % has been reported by Sharp for a triple junction (GaInP/GaAs/GaInAs) under one sun, and even 43.5% under 418 suns for the triple junction with dilute nitride (GaInP/GaAs/GaInNAs) developped by Solar Junction [3]. Consequently a solution for epitaxy of various materials, at low thermal budget and with industrial standard technique, would be a significant improvement. With the building blocks of silicon epitaxy, germanium epitaxy, direct growth of monocrystalline Si on GaAs or monocrystalline Ge on Si developped in our lab, RF-PECVD seems to be a good approach for those epitaxy challenges [5–8]. In this paper we will focus on the silicon homo-epitaxy.

	Institution & Research group	Epitaxy	Thick [µm]	Solar cell performance				Details	Ref.
				V_{oc} [mV]	J_{sc} [mA/cm²]	FF [%]	η [%]		
Exfoliation or etching	UNSW, Australia Wang et al. (1996)	-	47	698	37.9	81.1	21.5	Wafer chemical thinning, PERL cell	[9]
	AstroWatt inc., USA Rao et al. (2011)	-	25	590	30.2	70.0	12.5	Lift off: patented kerfless exfoliation technique from parent wafer	[10]
Epitaxial lift off	IPE, Germany Bergmann et al. (2002)	CVD, 1100°C	24.5 46.5	636 645	30.4 32.8	79.7 78.2	15.4 16.6	Lift off , transfer from porous silicon, random pyramids, epitaxial BSF	[11]
	ISFH, Germany Petermann et al. (2012)	CVD, 1100°C, 1µm/min	43	650	37.8	77.6	19.1	Lift off, transfer from porous silicon, random pyramids, PERC cell	[12]
Wafer equivalent approach	Fraunhofer ISE, Germany Rosenits et al. (2011)	CVD, 1100°C	50	645	32.7	78.2	16.5	Standard diffused emitter, no surface texture	[13]
	IMEC, Belgium K.Van Nieuwenhuysen et al. (2010)	CVD, 1100°C	20	621	33.2	78.0	16.1	Porous back reflector, BSF, epitaxial base & emitter, plasma surface texture	[14]
	NREL, USA Alberi et al. (2010)	HWCVD, 760°C	2	570	15.4	72.5	6.3	No surface texture	[15]
	LPICM, France R. Cariou et al.	RF-PECVD, 175°C	3.4	534	19.9	80	8.5	No surface texture	[7]

Table 1. Record efficiencies for thin film crystalline silicon solar cells based on different approaches: wafer thinning, epitaxy with subsequent lift off, and wafer equivalent approach. Note that device structure and absorber thickness may differ significantly for each group.

Table 1. summarizes the different approaches and results achieved for c-SiTF. The top down approach consisting of wafer thinning has proven to be effective: an efficiency of 21.5 % has been achieved for a 47 µm chemically thinned PERL cell [9], with excellent fill factor. But adding complex process steps with no material saving is not a viable solution. More recently, the AstroWatt company has patented a process to exfoliate several c-Si layers from a c-Si wafer [10], but solar cell results are still lagging behind. For the bottom up approach of silicon epitaxy followed by lift off and transfer to foreign substrates, promising results are already reported [11], [12]. The bottom up approach offers the possibility of cost saving through material reduction and wafer re-use. Even if the fabrication process cannot be implemented at the industrial scale yet, it is a proof of concept that less than 43 µm are enough to match wafer based efficiency. And finally, there is the wafer equivalent approach, in which the substrate is ideally an inexpensive and non-active seed layer for the epitaxial growth. Many groups are working in this field [7], [13–15]. In this paper, we report our state of the art 8.5% efficiency and 80 % FF for 3.4 µm epitaxial absorber in the wafer equivalent approach, with RF-PECVD epitaxy at 175°C.

For few micron thick epitaxial silicon solar cells, efficient light trapping is a crucial feature. Figure 1. Shows how much current can be collected under the assumptions: i) AM1.5 incident spectrum, ii) perfect antireflection coating and iii) 100% internal quantum efficiency. Bottom and right axes represent this ideal short circuit current (J_{sc}) versus wave-length for single pass absorption and different thicknesses. It is clear that with its indirect band gap, silicon cannot reach high short circuit current with a thin absorber. Top and left axes represent J_{sc} as a function of absorber thickness for three different absorption scenarios: i) single pass ii) X10 light trapping and iii) Yablonovitch limit corresponding to $4n^2$ enhancement. As an example, one can notice that a 3 µm thick epitaxial absorber leads to a maximum J_{sc} of 20.4, 35.5 and 37.7 $mA.cm^{-2}$ depending on the light trapping scenario. A X10 light trapping is something currently achieved in c-Si solar cells and new structural concepts based on nano-cone gratings [16] show that one can get very close to the Yablonovitch limit. In this context, c-SiTF seems to be a very promising solution for the future of silicon solar cells. Efficiencies close to 20 % for 3 µm epitaxial solar cell should be possible with advanced light trapping.

2.EXPERIMENT

Heavily boron-doped, (100)-oriented, c-Si wafers with a resistivity of 0.02-0.05 Ω.cm and a thickness of 525 µm were used as a substrate for the epitaxial growth, as well as providing the bottom electrical contact of the solar cell. We removed the native oxide from the c-Si by a 30 seconds dip in a 5%-diluted hydrofluoric acid solution, just before loading them into a standard (13.56 MHz) capacitively coupled RF-PECVD reactor [17]. Non-intentionally doped epitaxial Si layers of various thicknesses (0.9 µm, 1.7 µm and 2.4 µm) were deposited from the dissociation of a silane-hydrogen mixture and completed with the deposition of a standard (n+) a-Si:H emitter in the same PECVD reactor, without breaking vacuum. The substrate temperature was kept at 175°C throughout the deposition process. The area of the cells (2×2 cm^2) was defined by sputtering ITO through a shadow mask and evaporating Al grid contacts. Note that all the interfaces are flat and that no light-trapping scheme was applied to the devices. The undoped epitaxial layer was deposited by the dissociation of a 6% silane in hydrogen gas mixture under a total pressure of 2000 mTorr and an RF

power density of 60 mW.cm^{-2}, resulting in a deposition rate of 2 Å.s^{-1} (electrode spacing 17 mm). The n-type a-Si:H layer was deposited from the dissociation of 0.4% PH_3 in silane under a total pressure of 100 mTorr and an RF power of 6 mW.cm^{-2} resulting in a deposition rate of 0.5 Å.s^{-1} (electrode spacing 28 mm).

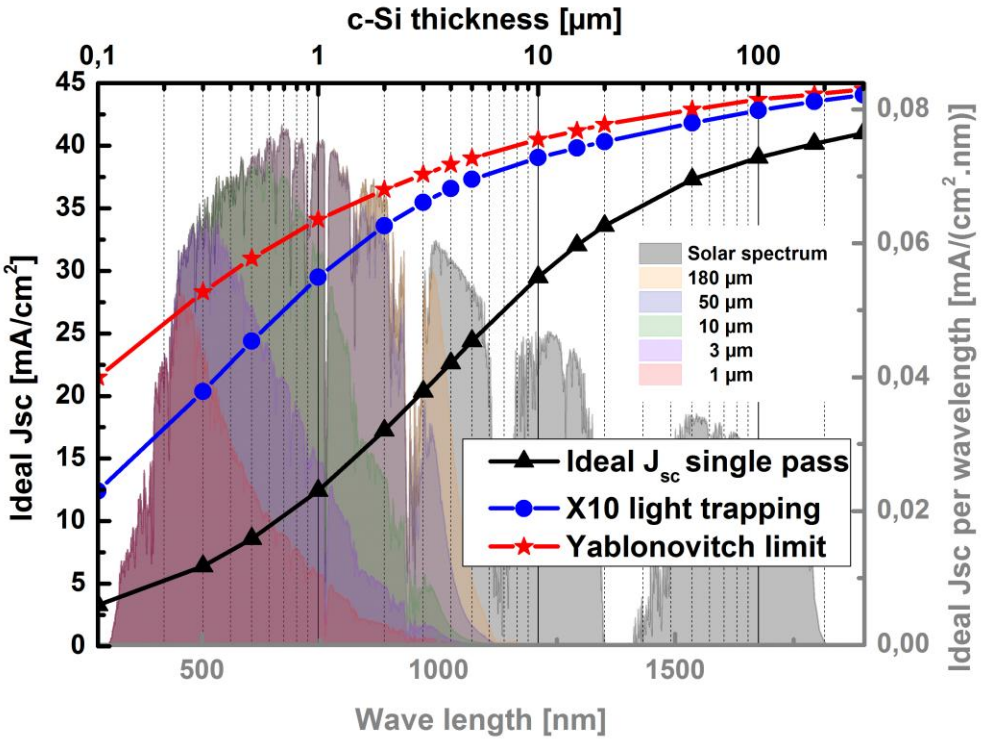

Figure 1. Bottom-X right-Y: ideal J_{sc} per wave length for a single pass absorption in different c-Si thicknesses. Top-X left-Y: Ideal J_{sc} as a function of c-Si thickness for: i) single pass absorption (triangles) ii) X10 light trapping (circles) iii) Yablonovitch limit [18], [19].

Layers are then characterized via spectroscopic ellipsometry (SE), using a phase modulated ellipsometer UVISEL from HORIBA Jobin-Yvon in the energy range 0.8 – 4.8 eV at 70° incident angle. Optical modeling and data analysis were done using DeltaPsi2 software. Crystal quality and detailed interfaces properties are investigated using JEOL 2010F transmission electron microscope (TEM) with a Schottky field emission gun operating at an acceleration voltage of 200 kV. I–V measurements under AM1.5 global spectrum illumination were carried out to determine the solar cell parameters.

3.RESULTS

Right side of Figure 2 shows the schematic stack of our epitaxial solar cell. The highly doped wafer is 525 µm thick, epi-Si layer thickness varies from 2 to 5 µm, and n+ a-Si:H emitter is typically 10 to 12 nm thick. The pseudo dielectric function of one sample measured by ellipsometry is shown on left part of Figure 2. The blue line corresponds to the fitting of the experimental data (red dots) with the optical model detailed in the graph. One can see the very good agreement between experiment and measurement. The inset zoom shows interference fringes appearing because of the

presence of a porous layer between the c-Si substrate and the epi-Si layer. They allow us to accurately determinate the epi-layer thicknesses. This epitaxial sample is perfectly fitted by a 100 % c-Si material of 4.2 µm with a 1 nm thick interface layer consisting of 60% of voids and 40% of c-Si. This non perfect interface can be attributed to our cleaning process which introduces a small roughness and leaves some oxide due to the short air exposure before loading into the reactor. The top n+ aSi:H layer (surface roughness) is modeled as a 4 nm thin layer with 37 % void fraction.

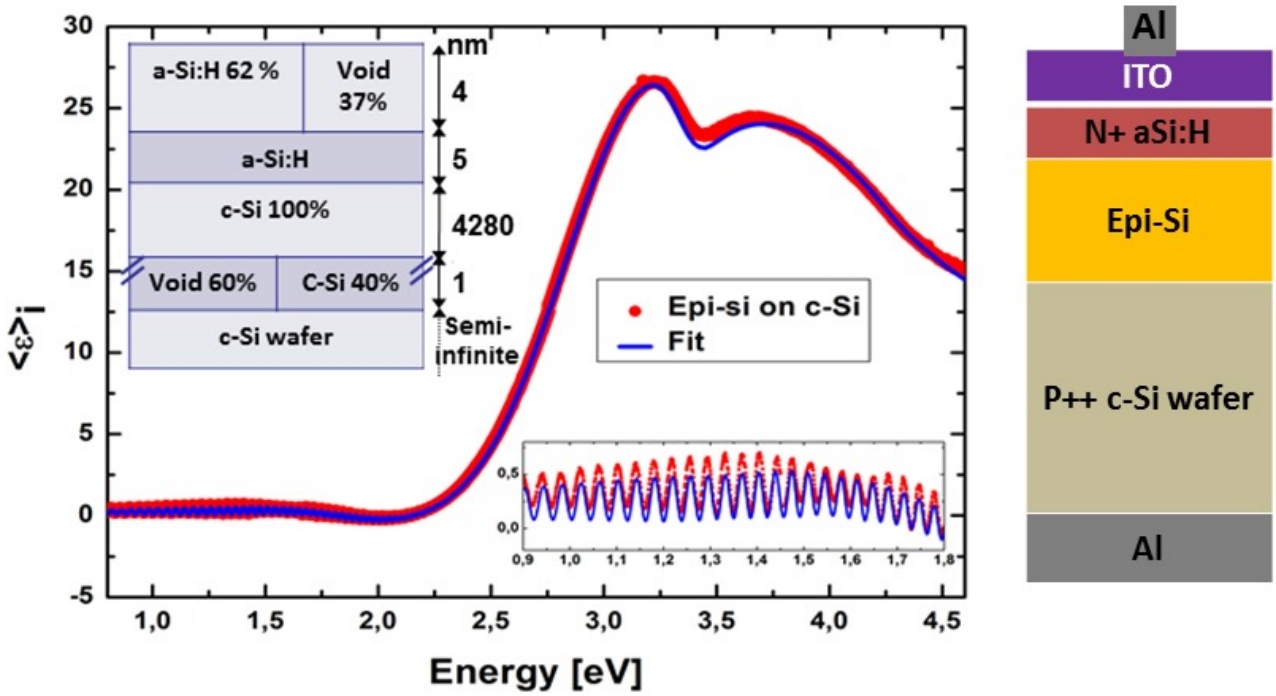

Figure 2. Right: Schematic representation of our epitaxial solar cell stack. Left: Ellipsometry measurement (red points) and corresponding fit (blue line) with the otpical model detailed in the graph. The inset provides a zoom on the low energy interference fringes.

For accurate material characterisation, crossection TEM analyses have been performed. Left side of Figure 3 shows the results of the TEM study: the whole stack c-Si wafer/epi-Si/a-Si:H is visible on the low magnification image, while a high resolution zoom on the wafer/epi-layer interface and on the top of the epi-layer are shown. The high crystal quality deduced from ellipsometry is confirmed here by the well defined points visible in the FFT picture corresponding to silicon family planes. The high resolution picture from the interface region reveals defects remaining and a roughness around 1 nm as modeled by ellispometry. Defects visible as darker spots in the bulk of the epi-layer are probably well passivated by the high hydrogen incorporated during epitaxial growth from the hydrogen-rich plasma environment. Indeed, a deposition temperature below 200°C allows hydrogen incorporation at around 1%, as revealed by SIMS. After 3.4 µm of epitaxial growth, the RMS roughness remains below 2 nm and the interface with the top a-Si:H is epi-regrowth free thanks to the use of a thin a-SiC:H alloy to disrupt epitaxial growth.

For conventionnal silicon epitaxy techniques (CVD, HWCVD, etc.) epitaxy breakdown is observed when depostion temperature is low: HWCD epitaxy growth between 550 and 620 °C leads to poly-Si, and below 550°C, it

breaks into amorphous after a few tens of nanometers [20]. Beeing able to grow Si monocrystal material at 175°C by RF-PECVD with no breakdown is the signature of a completely different growth mechanism. Instead of silane radicals as a main growth precursor, our hypothesis is that growth is mostly due to nanocrystals formed in the plasma . Their small size and high impact energy leads them to melt upon impacting on the (100) c-Si surface and the subsequent recrystallization at the c-Si/melted silicon interface [21], [22] leads to the epitaxial growth. Further investigations are ongoing for a better comprehension of this particular epitaxial growth mechanism.

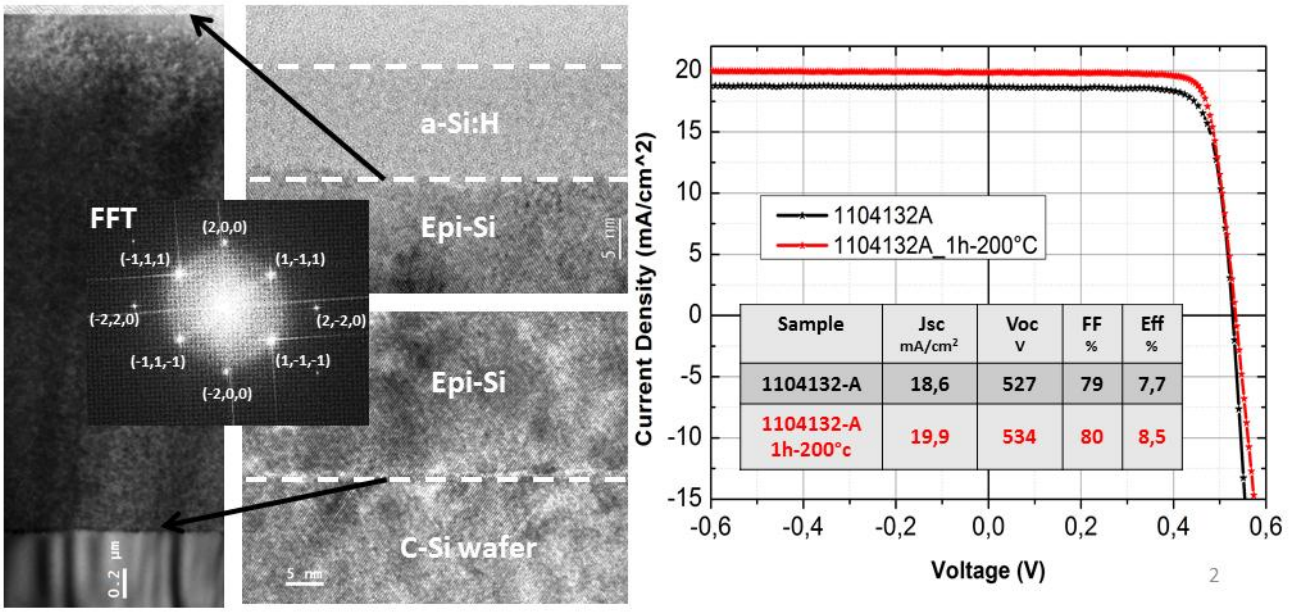

Figure 3. Left: cross section TEM picture of a thick Si epitaxial layer with zooms on top and bottom interfaces. Inset represents FFT of the epi-layer. Right: J(V) curve for a 3.4 µm epitaxial absorber with annealing effect.

Solar cell devices are made in the wafer equivalent approach, in which the epitaxial layer is used as an absorber layer. The J(V) curve under AM1.5G spectrum of our 3.4 µm absorber best solar cell is shown on the right part of Figure 3: detailed parameters are listed in the graph before and after a 200°c annealing step. V_{oc}, J_{sc} and FF benefit from the annealing step and we achieved the noteworthy 8.5% efficiency with a short circuit current of 20 mA.cm^{-2} and a fill factor of 80%. To our knowledge, this is the best result so far for that kind of cells in that thickness range. V_{oc} at 534 mV is still low compared to what can be expected but the poor c-Si/epi-Si interface is most probably responsible for this as discussed below.

4.SIMULATIONS

Device simulations have been carried out using the one dimensional detailed electrical-optical model "Amorphous Semiconductor Device Modeling Program (ASDMP) [23], [24]. Originally developed for modeling amorphous silicon based devices, it has been recently extended to simulate properly crystalline materials and HIT

devices. Based on Poisson's equation and the two carrier continuity equations under steady-state conditions for a given device structure, ASDMP yields the dark and illuminated J-V and QE characteristics. Similar to AMPS-1D [25] software code for the free and trapped charges, the recombination term, the boundary conditions and the solution technique, the program is ab-initio in its electrical part. The gap state model consists of the tail states and two Gaussian distribution functions to simulate the deep dangling bond states in the case of the amorphous layers, while in the epi-Si layer and c-Si substrate the tails are absent.

In the wafer equivale nt approach it is often assumed that carriers generated in the highly doped wafer do not contribute to the external current. However our simulations show that this assumption is not valid for small thicknesses. By comparing the absorption in the epi-layer (black open circles) and the EQE (black closed symbols) of the simulated 2.4 µm solar cell on Figure 4, one can see that EQE exceeds the absorption by almost 20 % at 550 nm. The same comparison for a 5 µm epitaxial cell (see red curves) reveals a much smaller discrepancy. Thus, for epi-layers ≳ 5 µm, the highly doped wafer does not have an active contribution in solar cell performances (S. Chakraborty et al., submitted to EPJPV, July 2012). Moreover, the contribution of the c-Si wafer decreases rapidly with epitaxial thickness and/or texturing.

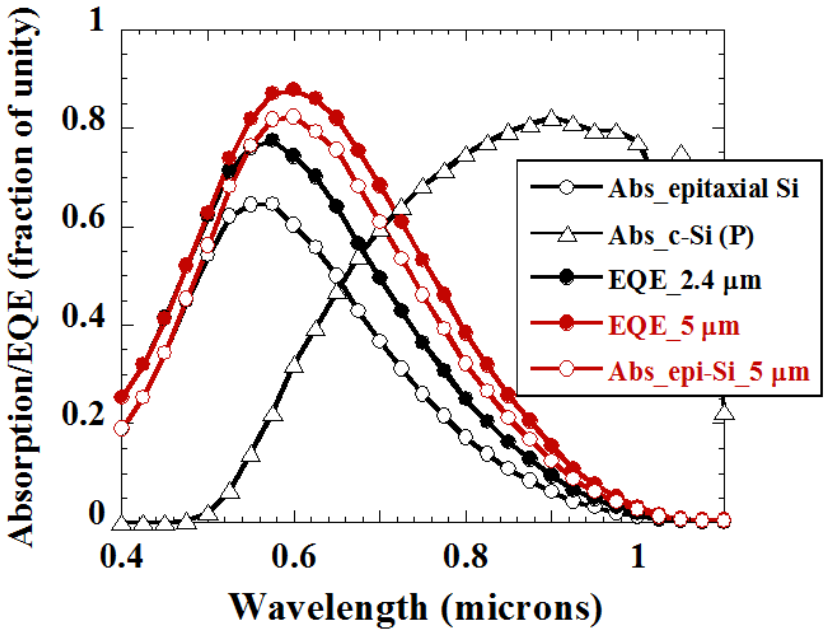

Figure 4. Simulated absorption (open symbols) and EQE (close symbols) of epitaxial silicon solar cells with 2.4 µm (black curves) and 5 µm (red curves) absorber.

The simulations based on real device performances allow us to extract some important material parameters and identify key points for improvement. The defect density (dangling bonds) is thus estimated to be around 10^{15} cm^{-3} for the bulk epitaxy before annealing and the density of defects at the interface between the c-Si wafer and the epi-Si layer to be in excess of 10^{12} cm^{-2}. Nevertheless, we could achieve a fill factor as high as 80% in our cells and this is probably linked to a dangling bond density reduced below 10^{14} cm^{-3} by the 200°C post annealing step. The relatively poor V_{oc} of

our devices can be attributed to the high density of recombination centers at epi-Si/c-Si interface. Our basic chemical cleaning process which includes air exposure before loading into reactor results in a non-oxide free interface. In-situ plasma cleaning for instance should lead to much cleaner wafer surface and a V_{oc} close to 600 mV can reasonably be expected, corresponding to an interface defect density below 10^{11} cm^{-2}. Moreover, doping of the epitaxial layer at the wafer interface is being studied in order to form a back surface field which can also reduce recombination at the interface with the c-Si wafer. Furthermore, modeling studies show that adding a front surface texturing to a 5 µm epitaxial layer with realistic values for the bulk defect density (i.e. 10^{14} cm^{-3}) and interface defect density (10^{11} cm^{-2}), an efficiency around 11 % can be achieved. Additional back surface texturing leads to an efficiency of 15 % for a 5 µm epitaxial silicon solar cell.

CONCLUSION

In this paper we have shown that provided an efficient light trapping scheme is applied, crystalline thin film epitaxial solar cells have the potential to reach high efficiency even for thicknesses below 10 µm. Substantial cost savings can be realized with this bottom up approach of epitaxy. Proof of silicon epitaxy at 175°C by RF-PECVD was shown by ellipsometry and TEM characterization. State of the art 8.5 % efficiency with 80 % fill factor for a 3.4 µm epitaxial wafer equivalent solar cell has been achieved. The high crystalline quality achieved by RF-PECVD together with hydrogen incorporation during epitaxial growth (defect passivation) is responsible for such promising solar cell device. Electro-optical modeling of the devices allowed us to extract material parameters and determine bottleneck issues. As a result 15% efficiency in 5 µm epi-layer, lift off and both side textured, should be achievable with our material parameters.

REFERENCES

[1] R. S. Ohl, « Light-Sensitive Electric Device », U.S. Patent 240266225-juin-1946.

[2] M. A. Green, « The path to 25% silicon solar cell efficiency: History of silicon cell evolution », *Progress in Photovoltaics: Research and Applications*, vol. 17, n°. 3, p. 183–189, 2009.

[3] M. A. Green, K. Emery, Y. Hishikawa, W. Warta, et E. D. Dunlop, « Solar cell efficiency tables (version 39) », *Progress in Photovoltaics: Research and Applications*, vol. 20, n°. 1, p. 12-20, déc. 2011.

[4] B. M. Kayes, H. Nie, R. Twist, S. G. Spruytte, F. Reinhardt, I. C. Kizilyalli, et G. S. Higashi, « 27.6% Conversion efficiency, a new record for single-junction solar cells under 1 sun illumination », in *2011 37th IEEE Photovoltaic Specialists Conference (PVSC)*, 2011, p. 000004 -000008.

[5] E. V. Johnson, G. Patriarche, et P. Roca i Cabarrocas, « Directional growth of Ge on GaAs at 175 °C using plasma-generated nanocrystals », *Appl. Phys. Lett.*, vol. 92, n°. 10, p. 103108, 2008.

[6] M. Moreno et P. R. i Cabarrocas, « Ultra-thin crystalline silicon films produced by plasma assisted epitaxial growth on silicon wafers and their transfer to foreign substrates », *EPJ Photovoltaics*, vol. 1, p. 6, 2010.

[7] R. Cariou, M. Labrune, et P. Roca i Cabarrocas, « Thin crystalline silicon solar cells based on epitaxial films grown at 165 °C by RF-PECVD », *Solar Energy Materials and Solar Cells*, vol. 95, n°. 8, p. 2260-2263, août 2011.

[8] R. Cariou, R. Ruggeri, S. Almosni, J. Nassar, et P. Roca i Cabarrocas, « Hetero-epitaxy of Germanium by RF - PECVD below 200°C: application to photovoltaics », *Submitted to APL*, 2012.

[9] A. Wang, J. Zhao, S. R. Wenham, et M. A. Green, « 21.5% Efficient thin silicon solar cell », *Progress in Photovoltaics: Research and Applications*, vol. 4, n°. 1, p. 55–58, 1996.

[10] R. A. Rao, L. Mathew, S. Saha, S. Smith, D. Sarkar, R. Garcia, R. Stout, A. Gurmu, E. Onyegam, D. Ahn, D. Xu, D. Jawarani, J. Fossum, et S. Banerjee, « A novel low cost 25 µm thin exfoliated monocrystalline Si solar cell technology », in *2011 37th IEEE Photovoltaic Specialists Conference (PVSC)*, 2011, p. 001504 -001507.
[11] R. B. Bergmann, C. Berge, T. J. Rinke, J. Schmidt, et J. H. Werner, « Advances in monocrystalline Si thin film solar cells by layer transfer », *Solar Energy Materials and Solar Cells*, vol. 74, n°. 1-4, p. 213-218, oct. 2002.
[12] J. H. Petermann, D. Zielke, J. Schmidt, F. Haase, E. G. Rojas, et R. Brendel, « 19%-efficient and 43 µm-thick crystalline Si solar cell from layer transfer using porous silicon », *Progress in Photovoltaics: Research and Applications*, vol. 20, n°. 1, p. 1-5, janv. 2012.
[13] P. Rosenits, F. Kopp, et S. Reber, « Epitaxially grown crystalline silicon thin-film solar cells reaching 16.5% efficiency with basic cell process », *Thin Solid Films*, vol. 519, n°. 10, p. 3288-3290, mars 2011.
[14] K. Van Nieuwenhuysen, M. R. Payo, I. Kuzma-Filipek, J. Van Hoeymissen, G. Beaucarne, et J. Poortmans, « Epitaxially grown emitters for thin film silicon solar cells result in 16% efficiency », *Thin Solid Films*, vol. 518, n°. 6, Supplement 1, p. S80-S82, janv. 2010.
[15] K. Alberi, I. T. Martin, M. Shub, C. W. Teplin, M. J. Romero, R. C. Reedy, E. Iwaniczko, A. Duda, P. Stradins, H. M. Branz, et D. L. Young, « Material quality requirements for efficient epitaxial film silicon solar cells », *Appl. Phys. Lett.*, vol. 96, n°. 7, p. 073502, 2010.
[16] K. X. Wang, Z. Yu, V. Liu, Y. Cui, et S. Fan, « Absorption Enhancement in Ultrathin Crystalline Silicon Solar Cells with Antireflection and Light-Trapping Nanocone Gratings », *Nano Lett.*, vol. 12, n°. 3, p. 1616-1619, 2012.
[17] P. Roca i Cabarrocas, « A fully automated hot-wall multiplasma-monochamber reactor for thin film deposition », *J. Vac. Sci. Technol. A*, vol. 9, n°. 4, p. 2331, juill. 1991.
[18] E. Yablonovitch et G. D. Cody, « Intensity enhancement in textured optical sheets for solar cells », *IEEE Transactions on Electron Devices*, vol. 29, n°. 2, p. 300 - 305, févr. 1982.
[19] M. A. Green, « Lambertian light trapping in textured solar cells and light-emitting diodes: analytical solutions », *Progress in Photovoltaics: Research and Applications*, vol. 10, n°. 4, p. 235–241, 2002.
[20] H. M. Branz, C. W. Teplin, M. J. Romero, I. T. Martin, Q. Wang, K. Alberi, D. L. Young, et P. Stradins, « Hot-wire chemical vapor deposition of epitaxial film crystal silicon for photovoltaics », *Thin Solid Films*, vol. 519, n°. 14, p. 4545-4550, mai 2011.
[21] P. Roca i Cabarrocas, R. Cariou, et M. Labrune, « Low temperature plasma deposition of silicon thin films: From amorphous to crystalline », *Journal of Non-Crystalline Solids*.
[22] P. Roca i Cabarrocas, K. h. Kim, R. Cariou, M. Labrune, E. v. Johnson, M. Moreno, A. T. Rios, S. Abolmasov, et S. Kasouit, « Low Temperature Plasma Synthesis of Nanocrystals and their Application to the Growth of Crystalline Silicon and Germanium Thin Films », *MRS Online Proceedings Library*, vol. 1426, p. null, 2012.
[23] P. Chatterjee, F. Leblanc, M. Favre, et J. Perrin, « A Global Electricai-Optical Model of Thin Film Solar Cells on Textured Substrates », *MRS Online Proceedings Library*, vol. 426, p. null, 1996.
[24] M. Nath, P. Chatterjee, J. Damon-Lacoste, et P. Roca i Cabarrocas, « Criteria for improved open-circuit voltage in a-Si:H(N)/c-Si(P) front heterojunction with intrinsic thin layer solar cells », *Journal of Applied Physics*, vol. 103, n°. 3, p. 034506-034506-9, févr. 2008.
[25] H. Zhu, A. K. Kalkan, J. Hou, et S. J. Fonash, « Applications of AMPS-1D for solar cell simulation », *AIP Conference Proceedings*, vol. 462, n°. 1, p. 309-314, mars 1999.