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## EPITAXIALLY GROWN CRYSTALLINE SILICON AS ELECTRON SELECTIVE CONTACT LAYER FOR CRYSTALLINE GERMANIUM TPV CELLS

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**ABSTRACT:** Crystalline germanium has been proposed as a cost-effective absorber for the fabrication of thermophotovoltaic (TPV) cells which require, among other technologies, the development of electron-selective contacts. In this work, we explore the deposition process of n-type high-quality crystalline silicon (c-Si(n)) on p-type crystalline germanium (c-Ge) substrates using Plasma-Enhanced Chemical Vapor Deposition (PECVD) to create c-Si(n)/c-Ge(p) heterojunctions that function as electron-selective contacts. Our analysis includes material characterization using Raman spectroscopy, X-ray diffraction, and Spectroscopic Ellipsometry measurements, confirming the crystalline nature of the epitaxially grown silicon layers. The interface quality of the heterojunction is studied by measuring the effective lifetime. The results demonstrate that the addition of a thin intrinsic amorphous silicon layer at the interface improves its passivation. Additional improvement is obtained after depositing a thin n-type amorphous layer on top of the c-Si(n), achieving a surface recombination velocity of 334 cm/s. This better passivation positively impacts both the open circuit voltage and the fill factor of 1x1 cm<sup>2</sup> finished devices, leading to an efficiency of 3.38%. The results suggest the potential of c-Si/c-Ge heterojunction for cost-effective c-Ge cells, with room for efficiency improvements through further optimization.

**Keywords:** epitaxial crystalline silicon, thermophotovoltaic, crystalline germanium, PECVD.

### 1 INTRODUCTION

Crystalline germanium (c-Ge) has a strong absorption up to 2 μm wavelength, which has been traditionally utilized in tandem and multijunction solar cells to boost their efficiency by harvesting infrared radiations [1]. Recently, c-Ge cells have been proposed as an affordable alternative to low-bandgap III-V semiconductors for thermophotovoltaic (TPV) applications, where the cell converts infrared thermal radiation into electricity [2-5]. Numerous efforts have been devoted to develop efficient carrier-selective contacts in c-Ge, since they are crucial in obtaining high-performance photovoltaic cells by separating the carriers photogenerated at the absorber with minimum recombination losses. Some examples are the homojunction-based carrier-selective contacts using thermal diffusion from spin-on dopant [2][3] or the application of laser firing process [4][5]. On the other hand, wide band gap semiconductors as carrier-selective contacts, forming heterojunction structures, offer potential advantages. In particular, the use of electron and hole selective contacts with an appropriate band alignment to the c-Ge absorber can lead to a significant reduction in carrier recombination. For this reason, several heterojunctions have been developed on c-Ge, including MoO<sub>x</sub> [6], hydrogenated amorphous silicon (a-Si:H) [7][8], InGaP [5], and microcrystalline silicon [9], among others.

Recently, ultrathin c-Ge epitaxial films were deposited on crystalline silicon (c-Si) wafers, acting as an effective buffer layer in tandem cells with comparable performance to the III-V layers growth on c-Ge substrates in terms of mismatching and crystallinity [10]. Simple Plasma-Enhanced Chemical Vapor Deposition (PECVD) was utilized in the process, opening a new perspective for low-cost epitaxial films, which have better doping efficiency, higher conductivity, higher

mobility, and lower optical absorption than their amorphous or microcrystalline counterparts. Moreover, PECVD has been demonstrated to produce high-quality epitaxial Si on GaAs, which has similar lattice parameter as c-Ge [11].

Therefore, this study aims to investigate epitaxial c-Si(n) grown by PECVD on p-type c-Ge wafers in order to develop high-quality electron-selective contacts. Firstly, we discuss the development and characterization of the c-Si(n) film on p-type c-Ge substrate. Secondly, we detailed strategies to improve the surface passivation of the c-Si(n)/c-Ge(p) heterojunction. Finally, devices were completed for further analysis of the interface quality. The findings of this study provide valuable guidance for developing highly efficient c-Ge TPV cells based on cost-effective and scalable manufacturing processes.

### 2 METHODOLOGY

This study utilizes 4-inch p-type c-Ge (100) wafers with a resistivity, doping, and thickness of 1.2 Ω·cm,  $2 \times 10^{15}$  cm<sup>-3</sup>, and 175 ± 15 μm, respectively. The c-Ge wafers are cleaned to obtain a H-terminated surface by dipping them into diluted hydrofluoric acid (HF, 1%) for one minute, followed by 30 seconds dip in DI water and 3 minutes dip in hydrochloric (HCl 32%):H<sub>2</sub>O water at 1:1 ratio. Firstly, we process the rear side of the wafers by depositing the dielectric stack (see the inset in Fig. 5), which consists of a H<sub>2</sub> plasma treatment followed by ~2 nm intrinsic amorphous silicon carbide (a-SiC<sub>x</sub>H(i)) layer deposited by PECVD at 400 °C. ALD is then used to deposit 50 nm aluminum oxide (Al<sub>2</sub>O<sub>3</sub>) layer at 200 °C. Finally, a 45 nm thick, close to the stoichiometric amorphous silicon carbide film (a-SiC) is deposited by PECVD at 370 °C. A post-annealing treatment at 360 °C is performed to fully activate the fixed charge of the

Al<sub>2</sub>O<sub>3</sub> layer, which is responsible for the field-effect surface passivation. This dielectric stack has resulted in the state-of-the-art passivation of the c-Ge wafers with a surface recombination velocity of 9 cm/s (see reference [12] for further details).

On the front side of the c-Ge wafer, the c-Si(n) thin film is deposited using a standard RF (13.56 MHz) PECVD reactor [13]. The H<sub>2</sub>, SiH<sub>4</sub>, and PH<sub>3</sub> flow rates are optimized as 350 sccm, 3 sccm, and 1 sccm, respectively. The optimum deposition temperature is set to 175 °C, and the electrode power was 12 W, with a pressure of 1,444 Torr. The developed c-Si film on the c-Ge is characterized by spectroscopic ellipsometry, Raman spectroscopy, and X-ray diffraction (XRD) measurements.

To get information about surface recombination at the c-Si(n)/c-Ge(p) interface, we use Sinton-WCT120 photoconductance tool to determine the dependence of effective lifetime ( $\tau_{eff}$ ) on excess carrier density. Considering negligible bulk recombination, i.e., bulk lifetime ( $\tau_b$ ) tending to infinity, and assuming that the rear side is well passivated by the dielectric stack a-SiC<sub>x</sub>H(i)/Al<sub>2</sub>O<sub>3</sub>/a-SiC with  $S_{rear} = 9$  cm/s, the front surface recombination ( $S_{front}$ ) between the c-Si(n)/c-Ge(p) wafer can be calculated using the following expression:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{S_{front}}{w} + \frac{S_{rear}}{w} \Rightarrow S_{front} = \left( \frac{w}{\tau_{eff}} - S_{rear} \right) \quad (1)$$

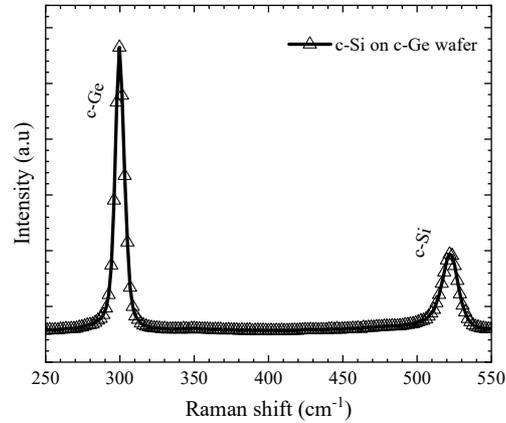
where  $w$  is the thickness of the wafer.

The heterojunction was studied under different configurations by introducing a thin a-Si:H film in the interface and on the highly doped c-Si(n). Finally, 1x1 cm<sup>2</sup> photovoltaic devices are completed by sputtering 80 nm indium tin oxide (ITO) film on the c-Si(n) layer using Magnetron system. After the ITO deposition, ~1 μm silver (Ag) metal grid was evaporated on the ITO surface. Finally, a ~1 μm Al mirror is evaporated at the rear side of the structure, followed by laser firing to create the local hole selective contact with a fixed processing area of 5%. Afterwards, these devices are characterized by measuring current density-voltage ( $J-V$ ) curves under air mass 1.5 global (AM1.5G) conditions.

### 3 RESULTS AND DISCUSSION

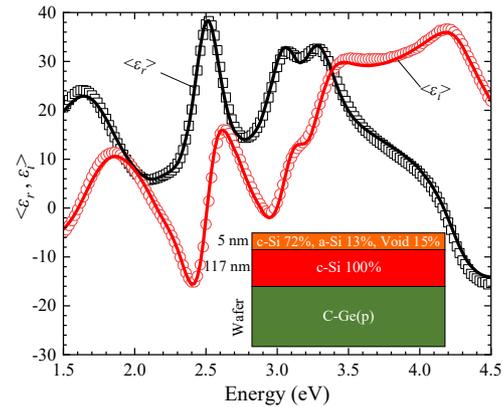
#### 3.1 Characterization of the c-Si(n) film

The structure of the deposited c-Si(n) film has been analyzed at room temperature using Raman spectroscopy. Fig. 1 shows the Raman spectroscopy measurements of the c-Si films deposited on the c-Ge wafer using the developed process. We can observe sharp Raman peaks in ~ 300 and 520 cm<sup>-1</sup>, which can be attributed to c-Ge and c-Si, respectively [14]. In particular, the sharp peak at ~520 cm<sup>-1</sup> indicates a dominant crystalline phase of silicon with negligible presence of amorphous phase whose Raman response is located at 480 cm<sup>-1</sup>. Additionally, the absence of a characteristic peak at 400 cm<sup>-1</sup> for Si-Ge phonon mode illustrates the lack of Si-Ge mixing material at the interface [15].



**Figure 1:** Raman spectroscopy of the c-Si(n) film on c-Ge(p) wafers.

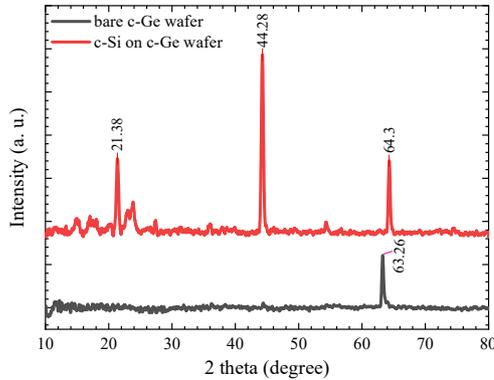
To confirm the crystalline quality of the silicon film, additional characterization is conducted using Spectroscopic Ellipsometry and XRD measurements. Regarding Spectroscopic Ellipsometry, Fig. 2 shows the real and imaginary parts of the pseudo-dielectric function  $\langle \epsilon_r \rangle$  and  $\langle \epsilon_i \rangle$  of the c-Si(n) thin film deposited on a c-Ge wafer. The experimental data is excellently fitted by considering a silicon layer of 117 nm consisting of 100% large grain c-Si and a top layer of ~5 nm with 72% of c-Si, 13% of a-Si, and 15% of voids, which can be interpreted as roughness on top of the c-Si layer. This result indicates the deposition of a high-quality c-Si(n) layer directly on the Ge wafer without forming any interfacial mixed Si-Ge layer, which agrees with the Raman spectroscopy analysis.



**Figure 2:** The real  $\langle \epsilon_r \rangle$  and imaginary  $\langle \epsilon_i \rangle$  part of the pseudo-dielectric function of c-Si(n) thin film deposited on a c-Ge wafer, where the symbol represents the experimental data while the line is the theoretical curve. The inset shows the layers used in the model to fit the experimental data with 117 nm c-Si bulk and 5 nm roughness.

Regarding XRD, Fig. 3 shows the XRD pattern of the c-Si(n) film on the c-Ge(p) wafer compared to the bare c-Ge wafer. The bare c-Ge wafer has a diffraction peak at a specific angle (2 theta) of 63.26°, representing the (100) orientation. After c-Si deposition, the c-Ge peak can still be observed, but two new peaks appear at

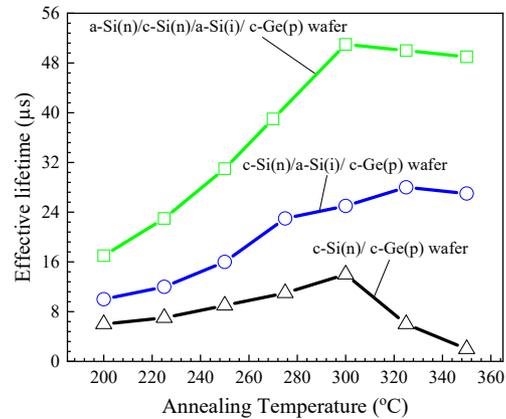
44.24° and 21.38°. Estimated by Bragg's Law, these two peaks can be attributed to c-Si planes of (111) and (100), respectively. This result again indicates no Si-Ge intermixing at the interface [10]. More importantly, the XRD spectrum exhibits sharp peaks, which also points to a high crystalline quality of the involved films, agreeing with the ellipsometry results.



**Figure 3:** XRD measurements of the c-Si(n) on c-Ge substrate (red line) and the bare c-Ge wafer (black line).

### 3.2 Surface passivation

The passivation quality of the heterojunction is characterized by quasi-steady-state photoconductance lifetime measurements, using a Sinton WCT-120, as described in the experimental section. Fig. 4 shows the effective lifetime as a function of cumulative annealing of 10 minutes in forming gas ( $N_2/H_2$ ) starting at 225 °C up to 350 °C. For the c-Si(n)/c-Ge(p) heterojunction, a low effective lifetime of 7  $\mu s$  is measured in the as-deposited state, which improves to 14  $\mu s$  after annealing at 300 °C. This short effective lifetime can most likely be attributed to the c-Si(n)/c-Ge(p) interface, which has a high defect density due to the mismatch in lattice parameters between c-Si ( $a = 0.5431$  nm) and c-Ge ( $a = 0.56575$  nm). In order to reduce the interface dangling bonds, a thin a-Si:H(i) layer ( $\sim 1$ nm) between the interface c-Si(n)/c-Ge(p) was introduced, resulting in a significant enhancement in the effective lifetime, as shown in Fig. 4. Suggesting an enhanced chemical passivation achieved by the presence of the intrinsic a-Si:H(i) layer. Therefore, a  $\sim 5$  nm n-type a-Si:H film was deposited on highly doped c-Si(n) to improve the effective lifetime, obtaining a maximum effective lifetime in the range of 50  $\mu s$ . This improvement is linked to the passivation of the ITO/c-Si(n) interface. Given the high quality of the c-Si(n) layer, minority carrier diffusion lengths longer than the layer thickness ( $\sim 100$  nm) are expected, which makes the ITO/c-Si(n) interface play a role in the recombination. Consequently, introducing a thin a-Si:H(n) layer can offer moderate passivation, effectively achieving a surface recombination velocity of 334 cm/s (calculated by equation 1) for the whole electron selective contact.

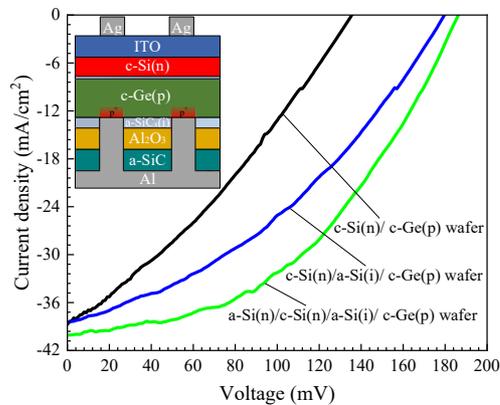


**Figure 4:** Effective lifetime measurements of three different configurations with c-Si(n) on c-Ge substrate as a function of the annealing temperature. For all samples, the rear side was coated by the dielectric stack a-SiC<sub>x</sub>:H(i)/Al<sub>2</sub>O<sub>3</sub>/a-SiC with a rear surface recombination velocities of 9 cm/s.

### 3.3 Device Characterization

Solar cell devices have been fabricated with three different configurations, as shown in the inset of Fig. 5 and as explained in detail in the methodology section. The current density-voltage ( $J$ - $V$ ) curves of the devices measured under AM1.5G illumination are shown in Fig. 5. The output performance of the cells followed a similar pattern to the passivation findings. Devices with c-Si(n)/c-Ge(p) heterojunction produce the lowest cell performance due to high surface recombination formed by a mismatch in the lattice characteristics of c-Si(n) and c-Ge(p). This mismatch resulted in a high interface state density and hampered overall device performance. The addition of the thin a-Si:H(i) film between the interface c-Si(n)/c-Ge(p) is critical in lowering the interface state density, resulting in an increase in cell performance, notably in improving the open-circuit voltage ( $V_{oc}$ ) and fill factor ( $FF$ ). Moreover, further improvement in the  $V_{oc}$  and  $FF$  is observed by depositing the a-Si:H(n) film on the c-Si(n). This additional step contributed significantly to the overall enhancement of device performance, which results in 3.38% ( $V_{oc} = 186.3$  mV,  $J_{sc} = 40.1$  mA/cm<sup>2</sup>,  $FF = 45.33\%$ ).

Although there is room for improvement (for example, reference [7] where a 5.26 % efficiency is reported with a-Si:H(n)/cGe(p) heterojunction), our findings highlight the potential of the utilization of high-quality c-Si(n) layers and the importance of a-Si:H(i) and a-Si:H(n) thin films at the interfaces to mitigate interface state density and improve the performance of the c-Ge cell. The results presented here pave the way for developing advanced Ge TPV cell technologies with higher conversion efficiencies and improved performance characteristics.



**Figure 5:** 1 Sun-illumination J-V curve of the developed c-Ge cell. A cross-section of the device structure is included in the inset.

#### 4 CONCLUSIONS

In summary, we have developed high-quality crystalline c-Si(n) layers on c-Ge(p) substrates. The crystalline quality of the silicon layers is confirmed by Raman spectroscopy, Spectroscopic Ellipsometry, and XRD characterization. Furthermore, the c-Si(n)/c-Ge(p) heterojunction solar cells were studied. It was found that the presence of the thin intrinsic a-Si:H(i) layer at the interface is beneficial to improve interface passivation, and further improvement is obtained when a thin a-Si:H(n) layer is deposited on c-Si(n). This better passivation positively impacts the  $V_{oc}$  and  $FF$  in finished devices. The reported efficiencies show room for improvement, but the results reported hereby suggest the potential of c-Si(n)/c-Ge(p) heterojunction for cost-effective c-Ge cells.

#### ACKNOWLEDGEMENT

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#### REFERENCES

- [1] S. P. Tobin, S. M. Vernon, C. Bajgar, V. E. Haven, L. M. Geoffroy and D. R. Lillington, *IEEE Electron Device Lett.*, Vol. 9 (1988) 2–4.
- [2] N. E. Posthuma, J. Van Der Heide, G. Flamand, and J. Poortmans, *IEEE Trans. Electron Devices*, Vol. 54 (2007) 1210–1215.
- [3] E.U. Onyegam, D. Sarkar, M. Hilali, S. Saha, R.A. Rao, L. Mathew, D. Jawarani, J. Mantey, M. Ainom, R. Garcia, W. James, S.K. Banerjee, *Sol. Energy Mater. Sol. Cells* 111 (2013) 206–211.
- [4] J. van der Heide, N. E. Posthuma, G. Flamand, W. Geens, and J. Poortmans, *Sol. Energy Mater. Sol. Cells* 93 (2009) 1810–1816.
- [5] J. Fernández, F. Dimroth, E. Oliva, M. Hermle, and A. W. Bett, *AIP Conf. Proc.*, Vol. 890 (2007) 190–197.
- [6] A. Alcañiz, G. López, I. Martín, A. Jiménez, A. Datas, E. Calle, E. Ros, L.G. Gerling, C. Voz, C. del Cañizo, R. Alcubilla, *Sol. Energy* 181 (2019) 357–360.
- [7] S. Nakano, Y. Takeuchi, T. Kaneko, and M. Kondo, in *Journal of Non-Crystalline Solids* 358 (2012) 2249–2252.
- [8] T. Kaneko and M. Kondo, *Jpn. J. Appl. Phys.* 50 (2011) 23–26.
- [9] B. Hekmatshoar, D. Shahrjerdi, S. W. Bedell and D. K. Sadana, 2012 38th IEEE Photovoltaic Specialists Conference, Vol. 1 (2012) 001590-001593.
- [10] M. Ghosh, P. Bulkin, F. Silva, Erik V. Johnson, I. Florea, D. Funes-Hernando, A. Tanguy, C. Renard, N. Vaissiere, J. Decobert, I. García, I. Rey-Stolle, P. Roca i Cabarrocas, *Sol. Energy Mater. Sol. Cells* 236 (2022) 111535.
- [11] R. Cariou, W. Chen, J-L. Maurice, J. Yu, G. Patriarche, O. Mauguin, L. Largeau, J. Decobert, P. Roca i Cabarrocas, *Sci Rep* 6 (2016) 25674 .
- [12] I. Martín, G. López, M. Garín, C. Voz, P. Ortega, and J. Puigdollers, *Surfaces and Interfaces* 31 (2022) 102070.
- [13] P. Roca i Cabarrocas, J. B. Chévrier, J. Huc, A. Lloret, J. Y. Parey, and J. P. M. Schmitt, *J. Vac. Sci. Technol. A9* (1991) 2331–2341.
- [14] W. S. Yoo, K. Kang, T. Ueda, T. Ishigaki, H. Nishigaki, N. Hasuike, H. Harima, M. Yoshimoto, C. S. Tan, *ECS J. Solid State Sci. Technol.*, 4 (2) (2015), P9–P15.
- [15] R. Cariou, J. Tang, N. Ramay, R. Ruggeri, and P. Roca i Cabarrocas, *Sol. Energy Mater. Sol. Cells* 134 (2015) 0927–0248.